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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/630,883	08/02/2000	Khosrow Golshan	82259/156	7954

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EXAMINER
CHANG, AUDREY Y

ART UNIT	PAPER NUMBER
2872	

DATE MAILED: 10/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/630,883	Applicant(s) GOLSHAN, KHOSROW	
	Examiner Audrey Y. Chang	Art Unit 2872	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-11,13-15,17-36 and 38-46* is/are pending in the application.

4a) Of the above claim(s) *23-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-10,13-15,17-22,31,33-36 and 38-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on *August 20, 2002* has been entered.

2. By this amendment, the applicant has amended claims 1, 11, 31 and 36.

3. Claims 1, 4-11, 13-15, 17-22, 31, 34-36, and 38-46 remain pending in this application.

4. Claims 23-30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 4.

Response to Amendment

5. The amendment filed on August 20, 2002 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: ***claims 1, 11, 31 and 36 have been amended*** to include the feature "the distance causing the selected interference" or "the distance being predetermined to selectively cause interference". The applicant is respectfully reminded that the distance does not cause the interference. The interference between two light beams is caused by the phase difference between the two light beams.

Applicant is required to cancel the new matter in the reply to this Office Action.

Drawings

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features recited in claims 1, 11, 31 and 36 concerning the *substrate*, the *patterned optical layer with a plurality of optical pathway or conduits* and the *interference region* must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. **Claims 1, 4-10, 11, 13-15, 17-22, 31, 33-36, and 38-46 are rejected under 35 U.S.C. 112, first paragraph,** as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The reasons for rejection based on the newly added matters are set forth in the paragraph above.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1 and 4-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase is representative of a Boolean logic output" recited in claim 1 is indefinite since it is not clear what is considered here as the "representation". Claims 4-10 inherit the rejection from their based claim.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 4-10, 11, 13-15, 17-22, 36, and 38-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Utaka et al (PN. 5,315,422) in view of the patent issued to Yang (PN. 5,239,173).

Utaka et al teaches an *interference type optical logic element* for controlling optical signal by light, i.e. an *optical processor*, that is comprised of

(1) a *substrate* (3) of a *first semiconductor material*, and

(2) a *patterned optical layer* (7) overlaying the substrate of a *second semiconductor material.*

Utaka et al teaches that the optical layer (7) is patterned with a plurality of *optical waveguides* serve as the *optical pathways or optical conduits* (I and II) with at least one of the optical pathways receives an optical input light signal (P_i) and at least one of the optical pathways configured to provide an optical output light signal (P_o), (please see Figures 2A, 2B, 3-5, 6A and 7-10). The input light signal propagates through the plurality of the waveguides or pathways to reach a region such that the light signals from the various waveguides interfere to each other wherein the interference causes the output light signal to perform a Boolean logical function, (please see columns 4-5). Utaka et al teaches that the

wavefronts of the light from the optical input signals via the optical conduits (I and II) intercept and interfere with each other at the region that two conduits meets, which is identified as interference region, (please see Figure 2A).

The input optical signals via either the optical conduits I or II, of Utaka et al, may be identified as the bias optical signal. Since as defined by the applicant the bias optical signal referred here is a *light signal* and Utaka et al also teaches that the input optical signals are provided as light signal, (P_0, column 3). Also the bias optical signal as one of the input optical signals must interfere with the other input signal to make the logic gate operable, this means the bias optical signal has to be **coherent** to the other input optical signal. The two input optical signals pass through the two conduits (I and II) of Utaka et al are generated as light input signals and are coherent to each other, it is therefore implicitly true that one of the signals can be identified as the bias optical signal.

Claims 1, 11 and 36 have been amended to make the two optical paths or optical conduits being separated by a distance at the entrance of the interference region. Yang in the same field of endeavor teaches an optical logic device that is comprised of at least two optical pathways or conduits for inputting input light signals into an interference region to allow the two light signals going through desired interference to perform the desired optical logic operation. Yang teaches that the optical pathways can be designed to have a distance separation between them at the entrances of the interference region, (please see Figures 5-6). It would then have been obvious to one skilled in the art to apply the teachings of Yang to modify the optical logic element of Utaka et al for the benefit of producing a different design for performing the same logic operations.

With regard to claims 4-8 and 38-42 Utaka et al teaches that the patterned optical layer may have two or three waveguides or pathways for receiving optical input light signal to perform various logical operations including AND, NAND, OR, XOR, NXOR. This reference (Utaka et al) does not teach explicitly to have the NOT logic function. Yang teaches that the optical logic device is capable to

perform NOT logic function. It would then have been obvious to one skilled in the art to modify the optical logic element of Utaka et al according to Yang for the benefit of adding NOT logic function to the logic operation of the optical logic element.

With regard to claims 9-10 and 44-45, Utaka et al teaches that the optical logic element is used as *optical processor* for processing and controlling optical signals. Utaka et al also teaches that a plurality of optical logic elements may be integrated such that a combination of basic logic functions (AND, OR and NOT) can be achieved to provide more complicated logic function such as NAND, XOR and NXOR. Although this reference does not teach explicitly to have the combined NOT and NAND functions such modification would have been obvious to one skilled in the art since it simply involves combining these elements for the purpose of performing the desired logic function.

With regard to claims 13-15, Utaka et al teaches that the patterned optical layer may have two or three waveguides or conduits for receiving optical input light signal to perform various logical operations such as AND, NAND, OR, XOR, NXOR. However this reference does not teach explicitly that the input light signals are biased. This feature is rejected for the reasons stated above. It also does not teach explicitly that the logical function is NOT. Yang teaches that the optical logic device is capable to perform NOT logic function. It would then have been obvious to one skilled in the art to modify the optical logic element of Utaka et al according to Yang for the benefit of adding NOT logic function to the logic operation of the optical logic element.

With regard to claims 17-20, Utaka et al teaches that the optical layer or the substrate may be formed by doped Gallium Arsenide, (please see column 1). However it does not teach explicitly that it may also be formed by doped silicon. However doped silicon is a very well known semiconductor material for making logic circuit in the art and since the specification fails to teach the criticality of having this particular material would overcome any problem in the prior art such modification would have been obvious matter design choice to one skilled in the art.

With regard to claims 21 and 22, Utaka et al teaches that a semiconductor DFB laser may be used as the light source to provide the input light signals, (please see Figure 8A and column 8).

With regard to claims 43 and 46, Utaka et al teaches that the optical logic element may perform logic functions such as NAND and XOR, (please see column 8).

13. Claims 31, and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Yang in view of Utaka et al.

Yang teaches a *binary data processor* for providing various logical functions wherein the processor comprises a coherent light source (11) for *providing light* through *light pipes* (41) serve as *the plurality optical pathways* and *slits* (13 and 14) serve as the *optical inputs* to a portion such that the light from the plurality of pathways or light pipes interfere with each other, (please see Figures 4 and 5, column 4). The interference pattern is transmitted via output light pipes (42) or fiber optic bundle (43) as the optical output light signal that may represent various logic functions such as AND, OR and NOT. **Claim 31 has been amended** to include the feature that a distance separation is set between the pluralities of pipes at the entrance of the interference regions. Figure 4 shows explicitly that at the entrances of the interference region the inputs and the light pipes are separated by a distance. The distance is implicitly predetermined to make the processor capable of performing the intended optical logic functions.

This reference has met all the limitations of the claims with the exception that it does not teach explicitly that the data processor is formed of optical transmission material patterned on a substrate material. It is extremely well known in the art to form optical logic circuit on a waveguide arrangement with patterned optical waveguides or pathways in a transmission optical material on a substrate material such is demonstrated by the teachings of ***Utaka*** et al with patterned optical layer (7) on a substrate (3), (please see Figure 2A). It would then have been obvious to one skilled in the art to apply the teachings of

Utaka et al to make the data processor with optical logic functions on a waveguide arrangement for the benefit of making it suited for desired applications.

Yang further teaches that logic circuit system having multiple logic steps can be constructed from combination of basic logic functions AND, OR and NOT. In Figure 6, Yang teaches a data processor system having a *cascaded series* of N optical processing steps that may include various combinations of the basic logic functions. Although this reference does not teach explicitly to have NOT AND (NAND) function and to have NOT and NOT AND function however since these functions are combinations of the basic logic functions, they are therefore either implicitly included or obvious modifications to one skilled in the art for the benefit of providing additional logic functions.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Audrey Y. Chang whose telephone number is 703-305-6208. The examiner can normally be reached on Monday-Friday (8:00-4:30), alternative Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cassandra Spyrou can be reached on 703-308-1637. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Audrey Y. Chang
Primary Examiner
Art Unit 2872

A. Chang, Ph.D.
October 18, 2002